PROJECT PROFILE

2T405: Chip/package-system co-design (CoSiP)

ENABLING TECHNOLOGIES FOR HETEROGENEOUS SYSTEMS

Partners:

Robert Bosch
CISC Semiconductor
DOCEA Power
Infineon Technologies
IRSEEM
MAGWEL
STMicroelectronics

Project leader:

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Key project dates:

Start: June 2008
End: December 2011

Countries involved:

Austria
Belgium
France
Germany

There is a constantly growing demand for complete system-in-package applications in the automotive and communications industries. Nevertheless, although a small number of chip developers may currently have the tools to combine the chip, package and printed-circuit board (PCB) design phases, it is not common practice for the various individual teams to collaborate. The goal of this MEDEA+ project is to develop a basic environment for the collaborative design of the complete chip-package system. The outcome of CoSiP is expected to create the ability to design more complex systems with a shorter time to market, fewer redesign cycles, better performance and more robust and reliable final products.

Future society will require compact system solutions in many fields, such as healthcare, pharmaceuticals, biochemistry, communications, mobility and transport, security, environmental control, weather forecasting, agriculture, recycling, education and entertainment. However, the realisation of these compact system solutions is challenged by the enormous complexity to be handled and the absence of generic technologies, methodologies and tools.

The so-called Moore's Law, describing the miniaturisation of the basic transistor components in integrated circuits (ICs) over time, has been the driving force of the microelectronics industry for more than 30 years. A dramatic change is now taking place in this trend. Although Moore's Law will continue to guide the semiconductor technology roadmap for digital functionalities such as computing power and data storage, there will be a growing need for analogue functions – such as radio-frequency (RF) communications, sensors and actuators – which enable the interaction of devices within the non-digital environment.

As these non-digital technologies do not scale in compliance with Moore's Law, they are collected together under the general title 'More than Moore' (MtM). The developing nanoelectronics era will be characterised by the emergence of compact system-in-package (SiP) devices, incorporating both 'More Moore' (MM) and MtM technologies.

Co-design methodology

In contrast to Moore's Law, there is not yet a technology roadmap for More than Moore. A key prerequisite for successful future developments of More Moore and especially More than Moore products using SiP technologies, as well as system-on-chip (SoC) components, is chip/package-system co-design methodology, data management and tooling.

The challenges of the absent co-design environment and tools are emphasised in the International Technology Roadmap for Semiconductors (ITRS).

Until now, normal practice in the SiP development world has been for the three major elements – namely chip, package and PCB – to be designed sequentially. Chip development is coupled neither with package nor board design. Package development is isolated both from chip design and PCB development. And the PCB development teams

only receive highly abstract information about the IC products.

In Europe, chip design is handled by three major players, one of which is also a leader in board design. Package-design tools for various applications are available although, typically, most developers have their own design flows based on specific tools. Currently, the leading electronic design automation (EDA) companies do not offer a common platform that combines all three design domains: chip, package and PCB.

A collaborative approach

Within the MEDEA+ 2T405 CoSiP project, two of the major European chipmakers – Infineon and STMicroelectronics – together with automotive electronics specialist Bosch, three small and medium-sized enterprises (SMEs) and one research institute from four European countries will collaborate to share their knowledge and expertise for the creation of an SiP chip/package/board co-design platform with the focus on European applications. This will strongly enhance the competitiveness of the nanoelectronics industry in Europe and satisfy the requirements of the European market and society.

The main challenge is to establish an environment in which people from different companies and disciplines work together to create a common open design platform for diverse design environments. At the same time, the project consortium will stay in touch with leading-edge technologies such as 3D and the large tool environment.

CoSiP will take care of the handling, interaction and interchange of results of various model views for the different abstraction layers for simulation such as the extraction of parasitic components of an SiP and back annotate them into a system simulation for crosstalk analysis.

Wherever necessary, hardware-dependent software modules will be integrated at various stages of the design flow to guarantee optimal system design space exploration and system verification for the target application. CoSiP will define the necessary accuracy for a given problem and develop adaptable component models for an optimised trade off between exactness and computational effort.

Selection of available software tools and the definition of an appropriate evaluation process for benchmark analysis will also be a part of the project.

A unified design environment

The MEDEA+ project aims to establish a design environment that supports the simple and reliable integration and simulation of proprietary and third-party subsystems to market tailored products. It will also create a unified SiP design platform – including 3D integration – that will be based on a new and optimised data model that fulfils all essential SiP design, integration and verification tasks.

The definition and implementation of a unified design environment supporting multi-physics and multi-technology design capabilities will also be on the schedule. At the same time, the project will also address the investigation and implementation of electrical, thermal and mechanical simulation as a prerequisite for the design flow. The validation and demonstration of the design platform based on different technology demonstration carriers, including virtual prototyping, is another key objective.

A further aim is the establishment of a European consortium of expertise in co-design consisting of EDA vendors, SMEs, academia, the microelectronics industry and other stakeholders.

Application of the open and configurable design environment established to the design flows with companies that already have their own procedures will be the cherry on the cake. Furthermore, the definition of standards to support interfaces between user environments will also help to enhance the design flows of those companies.

Strengthening European lead

The publication of the results of this MEDEA+ project will enable EDA vendors, SMEs and academia to adapt their own roadmaps to the needs of the European semiconductor industry.

At present, the EDA supplier market is heavily over-represented by US interests and is directly focused on the development of monolithic single-technology systems. CoSiP will strengthen the stance of European system designers and integrators and, at the same time, open up the tools and the market for European SMEs and universities.

By taking such a concerted effort, the European microelectronics industry will be able to retain and increase the lead it currently holds in SiPs and related markets.

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.